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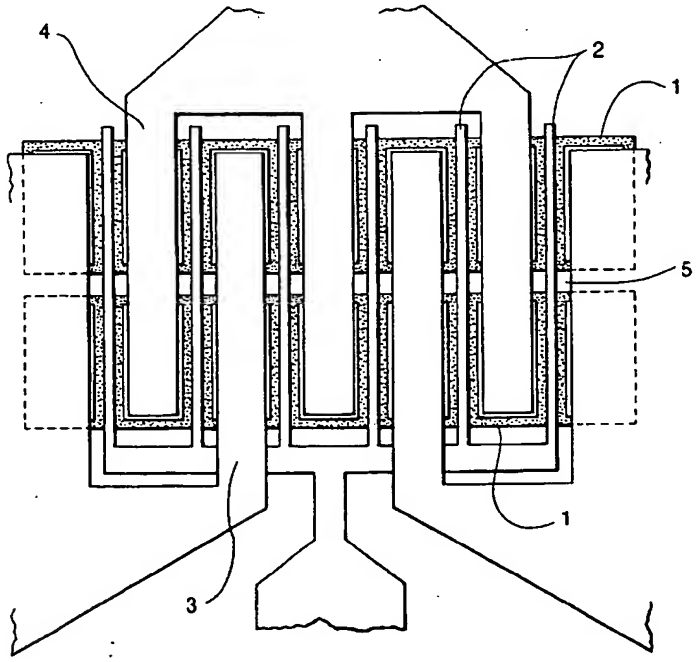
(54) Comb-shaped field effect transistor

(57) A semiconductor device has a structure in which pluralities of gate electrodes, drain electrodes, and source electrodes are alternately arranged in parallel with one another. The semiconductor device includes an isolation area formed in a direction perpendicular to the gate electrode so as to divide an active layer area formed on a semiconductor substrate into a plurality of active layer areas.

FIG. 3



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Description

BACKGROUND OF THE INVENTION

1. FIELD OF THE INVENTION

The present invention relates to a semiconductor device and, more particularly, to a high-output, high-frequency GaAs field effect transistor (FET).

2. DESCRIPTION OF THE PRIOR ART

To increase an output from a high-output FET, its gate width must be increased. For this purpose, a comb-shaped gate structure (inter-digital structure) in which gate fingers are formed parallel to each other is employed. In particular, a PHS (Plated Heat Sink) structure is employed in which a thin chip is used, and a thick metal layer is formed on the lower surface of the chip in order to cope with an increase in amount of heat generation with the increase in output from the element or device. In this structure, however, warping of the chip poses a problem.

Fig. 1 is a plan view showing conventional high-output FETs. In the structure shown in Fig. 1, pluralities of gate electrodes 2, source electrodes 3, and drain electrodes 4 are alternately aligned in parallel with one another on an active layer area 1 of the semiconductor device.

Although it is effective to increase the number of fingers in this manner so as to increase the device output, a too much increase in number increases the chip width, which, in turn, reduces the mechanical strength of the chip. In addition, the chip warpage increases due to the influence of heat in mounting. For this reason, the unit finger length must be increased to achieve a high output.

In the prior art, as shown in Fig. 1, the active layer area 1 is uniformly formed with respect to the gate fingers.

Although it is effective to increase the number of fingers as described above so as to increase the device output, the package capacitance undesirably increases, or the chip undesirably warps in assembling. In consideration of these problems, to achieve a high output, the unit finger length may be increased.

Warping of a chip originates from the PHS (Plated Heat Sink) structure in which a thin chip is used, and a thick metal layer is formed on the lower surface of the chip in order to cope with an increase in amount of heat generation with an increase in output from the element. That is, since the chip is thin, the chip warps even at room temperature due to the stress incurred by formation of the thick metal layer on the lower surface of the chip. When heat is applied in die bonding, the chip further warps, resulting in chip warpage. The stress of the warpage remains on the chip substrate, posing problems in reliability (e.g., the chip may crack in service due to a thermal shock upon an ON/OFF operation and may break in the worst case).

If the finger length is simply elongated, the decrement in thermal resistance with respect to a given DC power to be supplied becomes small, resulting in an increase in channel temperature.

Fig. 2 shows the relationship between a gate finger length L (μm), a thermal resistance Rθ (°C/W), and an increment ΔT (°C) in channel temperature. In Fig. 2, the finger length L (μm) is plotted along the abscissa, and the thermal resistance Rθ (°C/W) and the increment ΔT (°C) in channel temperature are plotted along the left and right sides of the ordinate, respectively.

Fig. 2 shows the thermal resistance Rθ obtained when the finger length is changed in a comb-shaped gate structure having 96 fingers, and the increment (ΔT) in channel temperature obtained when a DC power proportional to the gate width at that time is supplied. Note that the DC power is 1 W per unit gate width.

As for the relationship between the finger length L (μm) and the thermal resistance Rθ (°C/W) on the left side of the ordinate shown in Fig. 2, the thermal resistance can be reduced by increasing the finger length so as to increase the gate width. However, after the finger length reaches a certain value, the thermal resistance begins to decrease non-linearly.

On the other hand, in the relationship between the finger length L (μm) and ΔT (°C) on the right side of the ordinate, an increase in finger length L increases ΔT (°C). That is, when a DC power proportional to the gate width is supplied, ΔT undesirably increases with an increase in finger length L, resulting in a high channel temperature.

SUMMARY OF THE INVENTION

The present invention has been made in consideration of the above situation, and has as its object to provide a semiconductor device in which an increase in channel temperature can be suppressed even when the gate finger is elongated to expand the gate width.

To achieve the above object, according to the basic aspect of the present invention, there is provided a semiconductor device having a structure in which pluralities of gate electrodes, drain electrodes, and source electrodes are alternately arranged in parallel with one another, comprising an isolation area formed in a direction perpendicular to the gate electrode so as to divide an active layer area formed on a semiconductor substrate into a plurality of active layer areas.

In the basic aspect of the present invention, the isolation area is formed at, at least, one portion or at a plurality of portions between one and the other terminals of each electrode.

Further, in the basic aspect of the present invention, the isolation area has a width approximately twice a thickness of the semiconductor substrate.

In the structure of the present invention having the above aspects, the active layer area is divided into a

plurality of parts by the isolation area formed in the direction perpendicular to the gate electrodes. When this structure is used in a high-output FET having a comb-shaped gate structure in which gate fingers are formed parallel to each other, its output can be increased while the thermal resistance is reduced, and the channel temperature does not increase. More specifically, in an element having a comb-shaped gate structure in which a plurality of unit FETs are aligned parallel to each other, since the active layer area is divided into a plurality of parts by the isolation area formed in the direction perpendicular to the gate fingers, the heat diffusion path can be widened, thereby reducing the thermal resistance, and suppressing an increase in channel temperature. In addition, even when the gate finger is elongated, and the gate width is expanded in the high-output FET, an increase in channel temperature can be suppressed.

The above and many other advantages, features and additional objects of the present invention will become manifest to those versed in the art upon making reference to the following detailed description and accompanying drawings in which preferred structural embodiments incorporating the principles of the present invention are shown by way of illustrative example.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a plan view showing an example of a conventional semiconductor device;

Fig. 2 is a graph showing the relationship between the gate finger length, the thermal resistance, and the increment in channel temperature;

Fig. 3 is a plan view showing the first embodiment of a semiconductor device according to the present invention;

Figs. 4A to 4D are plan views sequentially showing the steps of manufacturing the first embodiment of the present invention;

Fig. 5 is a sectional view for explaining heat diffusion in an element;

Fig. 6 is a plan view showing the second embodiment of a semiconductor device according to the present invention; and

Fig. 7 is a graph showing the relationship between the number of isolation areas and the thermal resistance.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Preferred embodiments of the present invention will be described below with reference to the accompanying drawings.

Fig. 3 is a plan view showing a semiconductor device according the first embodiment of the present invention, and Figs. 4A to 4D are plan views showing the manufacturing steps, respectively.

In Fig. 4A, an n-type GaAs layer having an impurity concentration of 2×10^{17} cm^{-3} and a thickness of 0.3 μm is formed on a semi-insulating GaAs substrate 10 by an MBE method. This GaAs layer is patterned using a photoresist.

Oxygen or boron ions are selectively implanted in an area except for an active layer to form an isolation area 5. At this time, the isolation area 5 is formed to divide an active layer area 1.

The photoresist pattern is adjusted such that a width W of the isolation area 5 becomes twice the GaAs thickness (in general, 20 to 50 μm) in a chip form.

Next, in Fig. 4B, a photoresist film is applied on an insulating film which is deposited to a thickness of 300 to 400 nm and consists of, e.g., SiO_2. Then, the photoresist film is patterned. On the resultant structure, e.g., an aluminum film is vapor-deposited to a thickness of 500 nm to form gate electrodes 2 by a lift-off method.

As shown in Fig. 4C, a pattern is formed at source and drain electrode portions by using a photoresist film. AuGe/Ni is vapor-deposited to form ohmic electrodes 6 by a lift-off method.

Further, as shown in Fig. 4D, source electrodes 3 and drain electrodes 4 are formed. Then, Au-plated wiring metal layers are formed on the respective electrodes to complete a field effect transistor.

By the above steps, the structure shown in Fig. 3 can be obtained in which the isolation area 5 is formed in the active layer area 1, and the gate electrodes 2, the source electrodes 3, and the drain electrodes 4 are alternately arranged in parallel with one another.

With this structure, heat generated in the element diffuses into the isolation area 5 arranged in the active layer area 1, thereby reducing the thermal resistance Rθ.

Fig. 5 is a sectional view showing heat diffusion in the element. Heat flows 6 are indicated by arrows in the GaAs substrate 10 within the active layer area 1 and the isolation area 5.

Assuming that heat diffuses in the direction of 45° as shown in Fig. 5, the width W of the isolation area must be at least twice a thickness T of the GaAs substrate.

More specifically, it is preferable that the width W of the isolation area 5 be almost twice the thickness T (in general, 20 to 50 μm) of the GaAs substrate 10 of the chip. Note that the finger length becomes too large if the width W is set to be too large, and the thermal resistance Rθ becomes high if the width W is set to be too small. From this viewpoint, the width W is preferably almost twice the thickness T of the GaAs substrate 10.

Fig. 6 shows the second embodiment of the present invention.

Fig. 6 shows a structure in which isolation areas 5 are formed in an active layer area 1, and pluralities of gate electrodes 2, source electrodes 3, and drain electrodes 4 are alternately arranged parallel to each other. The isolation areas 5 are formed at two portions in the active layer area 1.

Similarly, the thermal resistance Rθ can be further reduced by arranging isolation areas 5 at a plurality of portions.

Fig. 7 shows the relationship between the number N of isolation areas and the thermal resistance Rθ. The number N of isolation areas is plotted along the abscissa, and the thermal resistance Rθ (°C/W) is plotted along the ordinate.

As shown in Fig. 7, for a given gate width, the thermal resistance Rθ is reduced with an increase in number N of isolation areas. Accordingly, an increase in channel temperature can be suppressed. Note that, in Fig. 7, the gate width is 28.8 mm, and the number of fingers is 96.

Claims

1. A semiconductor device having a structure in which pluralities of gate electrodes, drain electrodes, and source electrodes are alternately arranged in parallel with one another, comprising: an isolation area formed in a direction perpendicular to said gate electrode so as to divide an active layer area formed on a semiconductor substrate into a plurality of active layer areas.

2. A device according to claim 1, wherein said isolation area is formed at, at least, one portion or at a plurality of portions between one and the other terminals of each electrode.

3. A device according to claim 2, wherein said isolation area has a width approximately twice a thickness of said semiconductor substrate.

FIG. 1
PRIOR ART

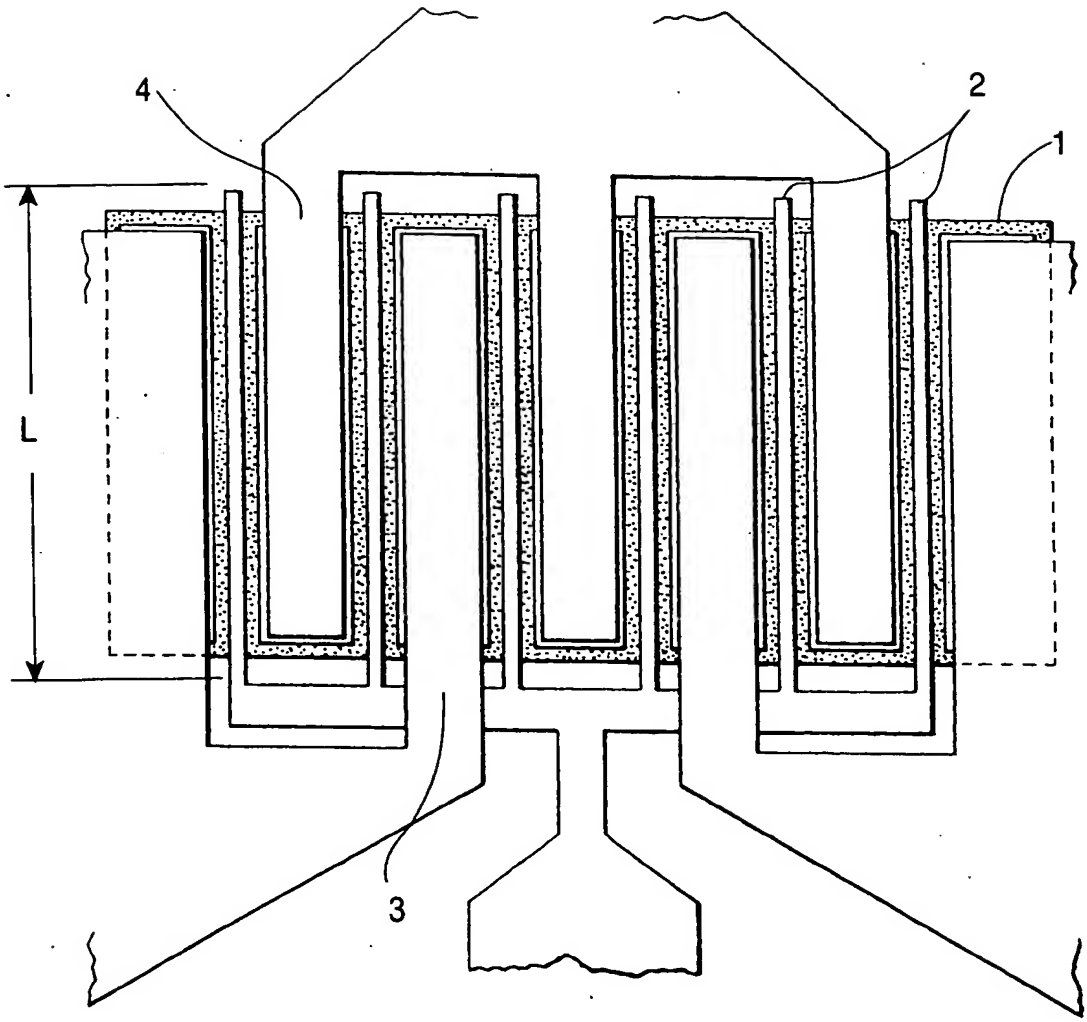


FIG. 2
PRIOR ART

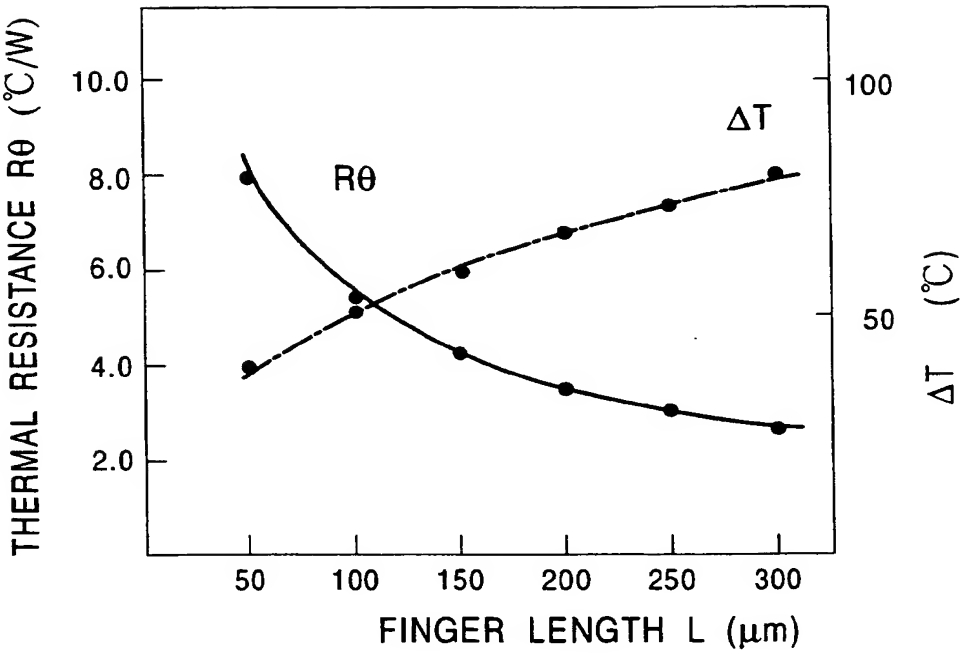


FIG. 3

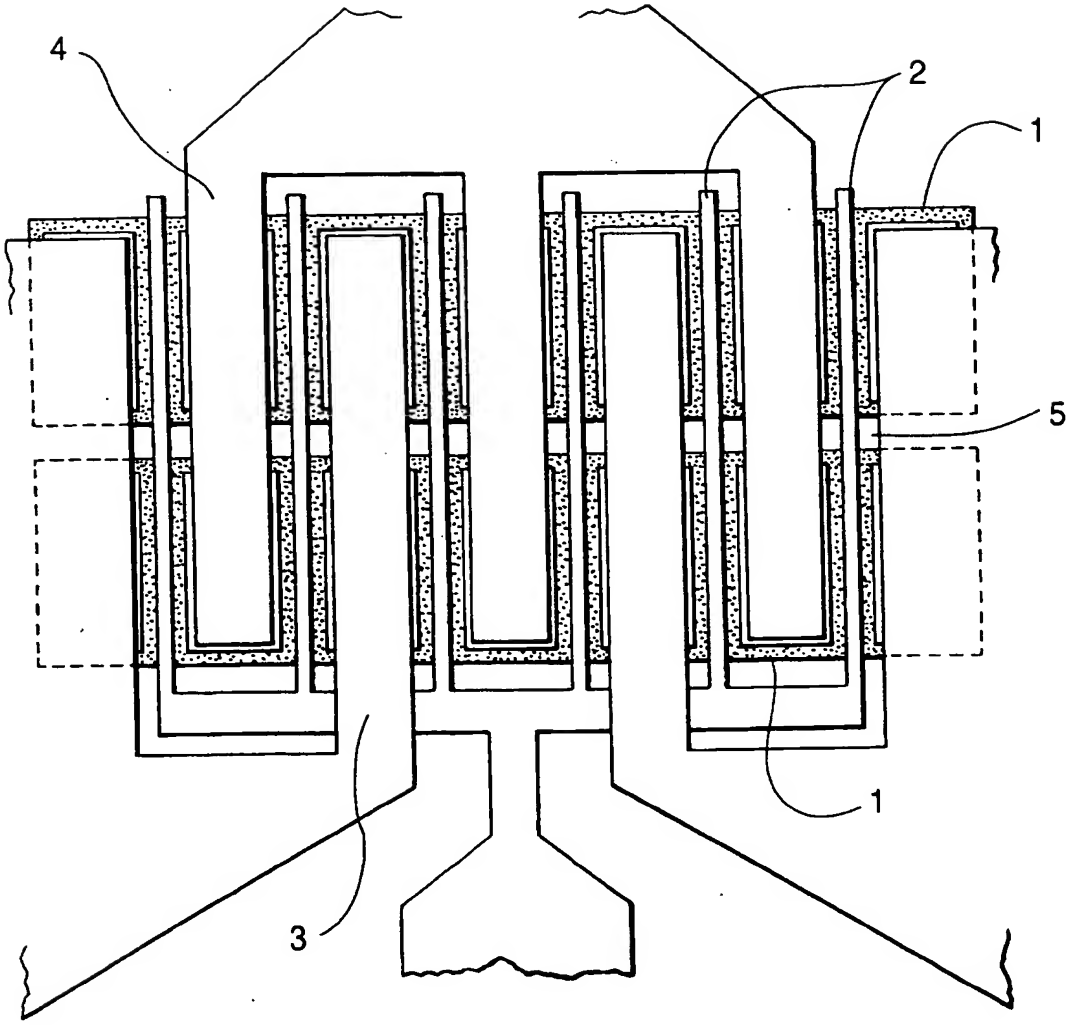


FIG. 4A

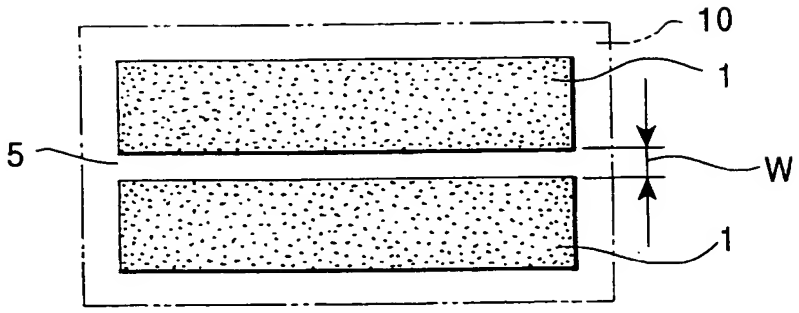


FIG. 4B

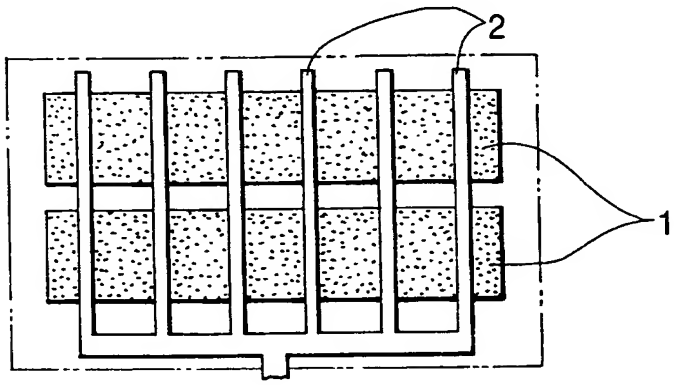


FIG. 4C

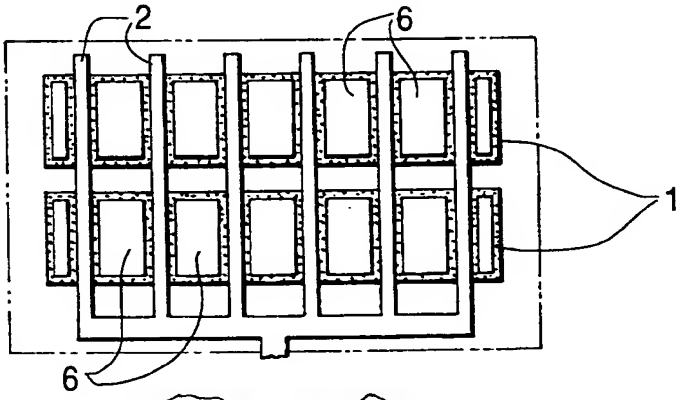


FIG. 4D

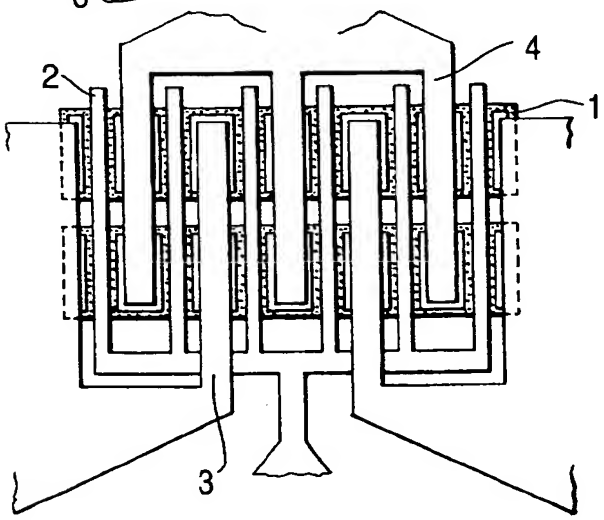


FIG. 5

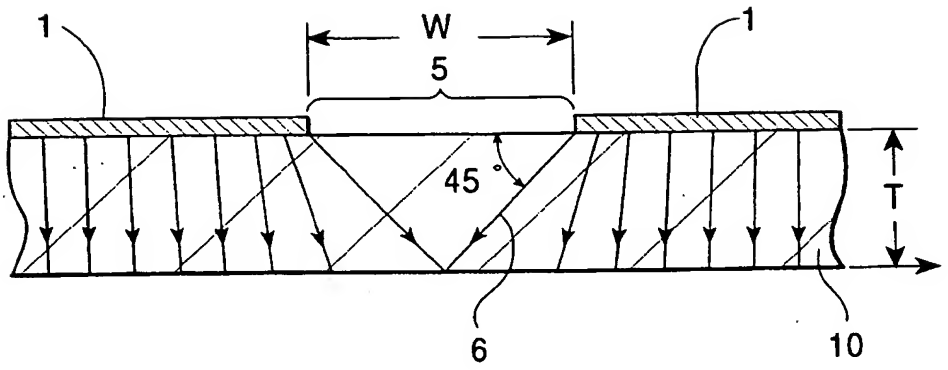


FIG. 6

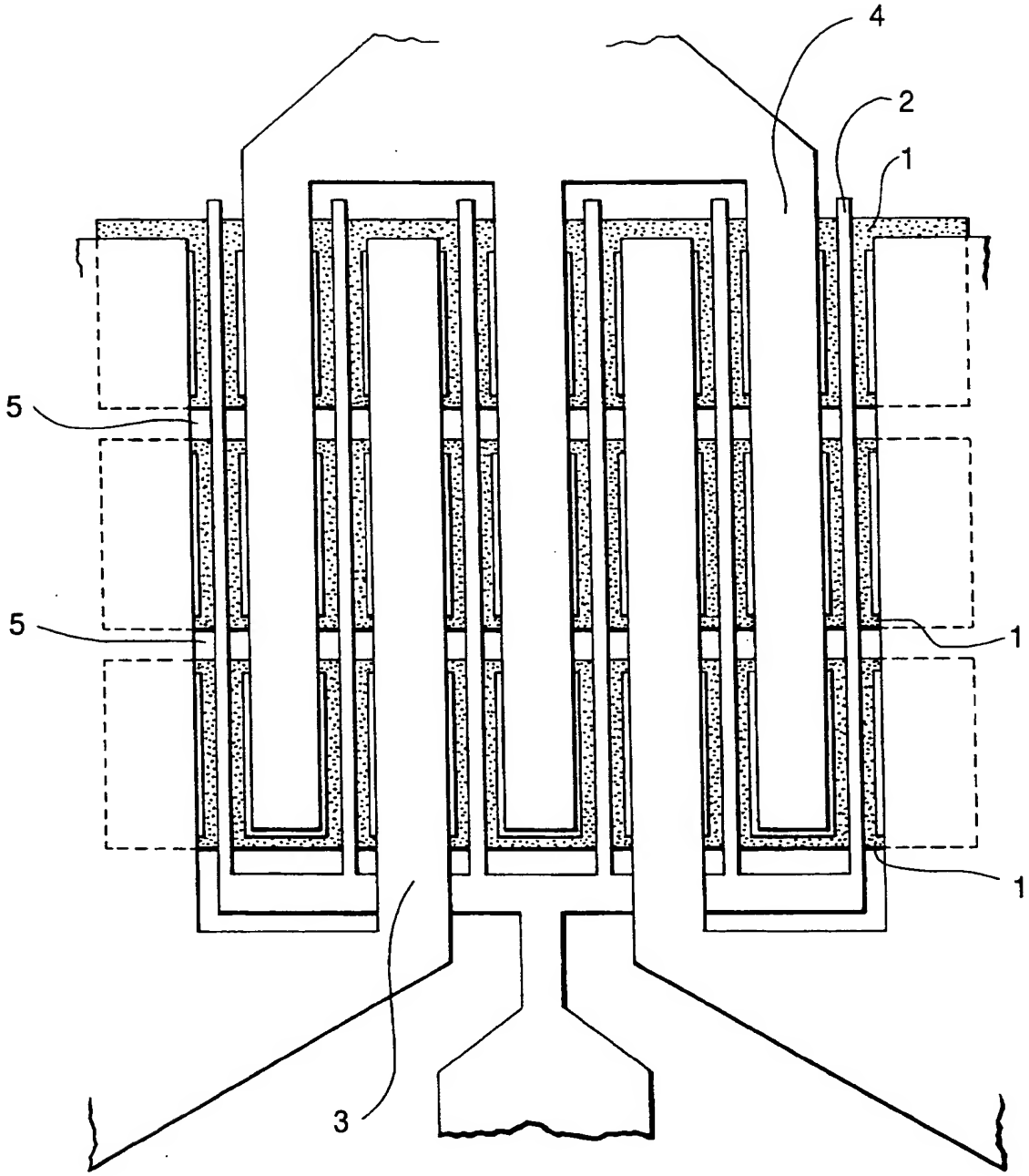
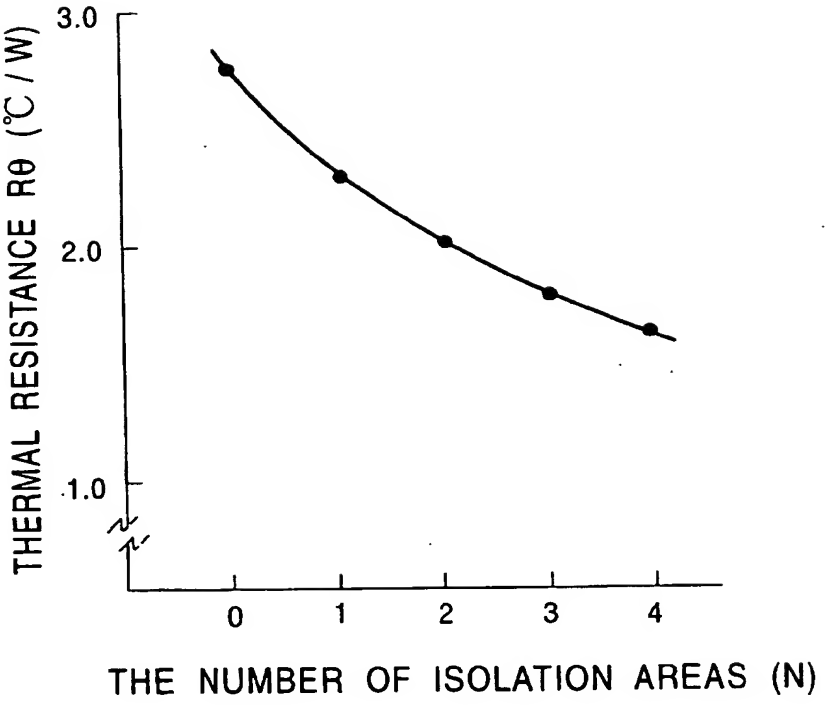


FIG. 7



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EUROPEAN SEARCH REPORT

Application Number
EP 96 10 1606

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	PATENT ABSTRACTS OF JAPAN vol. 006, no. 264 (E-150), 23 December 1982 & JP-A-57 160148 (TOKYO SHIBAURA DENKI KK), 2 October 1982,	1,2	H01L29/10 H01L23/66
A	* the whole document *	3	
A	EP-A-0 373 803 (RAYTHEON CO) 20 June 1990 * figures 1,3,4 *	1-3	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)

H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
BERLIN	20 May 1996	Juhl, A

CATEGORY OF CITED DOCUMENTS

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